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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/936,032 | 03/11/2002 | Michael Nicolaidis | 514842000100 | 9437 |

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Erwin J Basinski Esq
BASINSKI & ASSOCIATES
113 San Nicolas Avenue
Santa Barbara, CA 93109

| EXAMINER | |
|---|---|
| GANDHI, DIPAKKUMAR B | |
| ART UNIT | PAPER NUMBER |
| 2138 | |

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/936,032 | NICOLAIDIS, MICHAEL | |
| | Examiner | Art Unit | |
| | Dipakkumar Gandhi | 2138 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *06 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-5,9,10 and 12* is/are allowed.

6)☒ Claim(s) *6-8 and 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

***Response to Amendment***

1. Applicant's amendment including amended claims and Request for continued Examination (RCE) filed on 3/6/2006 has been entered.

***Specification***

2. The disclosure is objected to because of the following informalities:

In the amendment to the specification filed on 3/6/2006 the following items should be corrected.

- "U.S. patent application Ser. No. 10/268,686 filed November 1, 2002" should be corrected to -- U.S. patent application Ser. No. 10/286,686 filed November 1, 2002--.
- "U.S. patent application Ser. No. 10/379,126 filed March 3, 2003, titled "A Reconfiguration Device for a Faulty Memory" should be corrected to -- U.S. patent application Ser. No. 10/379,126 filed March 3, 2003, titled "Programmable test for memories"--.

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 6, 7, 8 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakao (JP 56140722 A).

Nakao anticipates claim 6.

Nakao teaches a circuit protected against transient disturbances, the circuit comprising: a combinatory logic circuit having at least one output; a first flip-flop rated by a clock, the first flip-flop being connected to receive said output; a second flip-flop connected to said output and rated by the clock delayed by a predetermined duration; and a circuit for analyzing outputs of the flip-flops, the analysis circuit indicating an error if the flip-flop outputs are different (abstract, fig. 3, 6, Nakao).

- Nakao anticipates claim 7.

Nakao teaches the protected circuit wherein the second flip-flop is controlled by the same clock as the first flip-flop, but by a different edge or level of this clock (abstract, fig. 3, 6, Nakao).

- Nakao anticipates claim 8.

Nakao teaches a circuit protected against transient disturbances, the circuit comprising: a combinatory logic circuit having at least one output; a first flip-flop rated by a clock, the first flip-flop being connected to receive said output; a second flip-flop rated by the clock and receiving said output delayed by a predetermined duration; and a circuit coupled to receive outputs of the first flip-flop and the second flip-flop, for analyzing the flip-flop outputs, the analysis circuit indicating an error if the flip-flop outputs are different (abstract, fig. 3, 6, Nakao).

- Nakao anticipates claim 11.

Nakao teaches the protected circuit further comprising: a third flip-flop rated by the clock and receiving said output delayed by twice the predetermined duration; wherein the analysis circuit is further coupled to receive an output of the third flip-flop (abstract, fig. 3, 6, Nakao).

***Allowable Subject Matter***

5. Claims 1-5, 9-10, 12 are allowed.

6. The following is an examiner's statement of reasons for allowance:

The present invention pertains to digital circuits insensitized to external disturbances, especially to localized disturbances coming in particular from heavy ion bombardments.

The claimed invention in claim 1 recites features such as: "a circuit protected against transient disturbances, the circuit comprising: a combinatory logic circuit having at least one output; a means for generating an error control code for said at least one output; and a memory element coupled to said means for generating an error control code and coupled to said combinatory logic circuit so as to receive the at least one output and the error control code, the memory element being controlled by the means for generating an error control code to be transparent when the error control code indicates that no transient disturbance has occurred, and to keep the state of said at least one output unchanged when the error control code indicates that a transient disturbance has occurred."

The prior art of record (Helm et al. US 5,072,450) teach that the local memory 16 includes a conventional parity check circuit 13 which, as a data word is read from the memory 16 and sent to the CPU 12, generates one or more parity bits for the word and compares them to the parity bits stored with the word. The parity bits generated by the circuit 37 are normally identical to the stored parity bits, and the parity check circuit 37 thus normally outputs a logic low voltage on its output line 38 to indicate that no error has been detected. On the other hand, if the parity bits generated by the circuit 37 are different from the stored parity bits, then an error has occurred and the circuit 37 produces a logic high voltage on its output line 38 to indicate the presence of an error (figure 1, col. 3, lines 20-33, Helm et al.).

Byers et al. (US 5,416,362) teach that the present invention overcomes the disadvantages found in the prior art by providing a single enable line to provide signal transparency to a master/slave flip-flop. When the line is enabled the flip-flop macro is transparent and when the line is disabled the macro returns to the latching state as in a conventional bistable multivibrator (col. 1, line 64 to col. 2, line 2, Byers et al.).

Stewart et al. (US 4,464,754) teach a memory system in which two or more memory modules containing the same information have their respective data outputs connected to the same data line. Each module includes means for checking the parity of the data being read-out at its output and in the event of a parity error indication effectively disconnects its output from the data line (abstract, Stewart et al.).

However, the prior arts of record do not teach a circuit protected against transient disturbances, the circuit comprising: a combinatory logic circuit having at least one output; a means for generating an error control code for said at least one output; and a memory element coupled to said means for generating an error control code and coupled to said combinatory logic circuit so as to receive the at least one output and the error control code, the memory element being controlled by the means for generating an error control code to be transparent when the error control code indicates that no transient disturbance has occurred, and to keep the state of said at least one output unchanged when the error control code indicates that a transient disturbance has occurred.

Hence, the prior arts of record do not anticipate nor render obvious the claimed inventions. Thus, claim 1 is allowable over the prior arts of record. Claims 2-5 are allowed because of the combination of additional limitations and the limitations listed above.

- The claimed invention in claim 9 recites features such as: " a circuit protected against transient disturbances, the circuit comprising: three identical logic circuits, wherein each of the logic circuits is preceded by a two-input memory element respectively receiving outputs of the two other logic circuits as the memory element's inputs, each memory element being provided to be transparent when its two inputs are identical, and to keep its state unchanged when the two inputs are different."

The prior art of record O'Lear (US 3,904,891) teaches a logic circuit for the transfer of true and complement binary digital bits of information that employs "single rail" techniques to eliminate several elements required in "double rail" logic circuits (abstract, O'Lear). O'Lear teaches that the second logic circuit illustrated in FIG. 2 comprising the elements 20a through 25a represent a second identical embodiment of the logic circuit of the present invention as it may be connected in parallel in a typical equipment to provide the true and complement transfer of multiple digital data (fig. 2, col. 7, lines 23-28, O'Lear).

Byers et al. (US 5,416,362) teach that the present invention overcomes the disadvantages found in the prior art by providing a single enable line to provide signal transparency to a master/slave flip-flop. When the line is enabled the flip-flop macro is transparent and when the line is disabled the macro returns to the latching state as in a conventional bistable multivibrator (col. 1, line 64 to col. 2, line 2, Byers et al.).

Stewart et al. (US 4,464,754) teach the memory system of FIG. 1 includes 8 sets (i=8) of two memory chips (Mij), where M identifies a memory chip, i the chip set, and j the chip within a set. Two chips (e.g. M11 and M12; - - - M81 and M82) are shown per set for ease of illustration. However, more than two chips could be used per set to increase the system reliability and the number of errors that can be detected and corrected). The data input (Iij) of each chip is connected to its data output (Oij) and the I/Oij terminals of the chips of a set are connected to the same data bus line DBi. Information to be written into each set of chips is applied to the data bus lines by a microprocessor or other source (not shown). Consequently, the same information is written into each chip of a set and, assuming error free operation, the same information should be read-out from each chip of a set. Consequently, barring any error or

defect, each chip of a set stores an identical copy of the data stored in the other chips of a set (col. 1, line 61 to col. 2, line 10, Stewart et al.).

However, the prior arts of record do not teach a circuit protected against transient disturbances, the circuit comprising: three identical logic circuits, wherein each of the logic circuits is preceded by a two-input memory element respectively receiving outputs of the two other logic circuits as the memory element's inputs, each memory element being provided to be transparent when its two inputs are identical, and to keep its state unchanged when the two inputs are different.

Hence, the prior arts of record do not anticipate nor render obvious the claimed inventions. Thus, claim 9 is allowable over the prior arts of record. Claim 10 is allowed because of the combination of additional limitations and the limitations listed above.

- The claimed invention in claim 12 recites features such as: "a circuit protected against transient disturbances comprising: a combinatory logic circuit having at least one output; a circuit for generating an error control code for said at least one output, said circuit for generating an error control code selected from a group of circuits consisting of a parity generation circuit and a circuit that is a duplicate of the combinatory logic circuit; and a memory element coupled to said circuit for generating an error control code and to said combinatory logic circuit, the memory element being controlled by the control code generation circuit to be transparent when the control code is correct, and to keep its state when the control code is incorrect; wherein said control code is correct when a parity generation circuit is used and when the output from the parity generation circuit is inactive, said control code being incorrect when the output from the parity generation circuit is active, and wherein said control code is correct when a duplicate of the combinatory logic circuit is used and when the out put from the duplicate of the combinatory logic circuit is identical to the output of the combinatory logic circuit, said control code being incorrect when the output from the duplicate of the combinatory logic circuit is not identical to the output of the combinatory logic circuit."

The prior art of record (Helm et al. US 5,072,450) teach that the local memory 16 includes a conventional parity check circuit 13 which, as a data word is read from the memory 16 and sent to the CPU 12,

generates one or more parity bits for the word and compares them to the parity bits stored with the word. The parity bits generated by the circuit 37 are normally identical to the stored parity bits, and the parity check circuit 37 thus normally outputs a logic low voltage on its output line 38 to indicate that no error has been detected. On the other hand, if the parity bits generated by the circuit 37 are different from the stored parity bits, then an error has occurred and the circuit 37 produces a logic high voltage on its output line 38 to indicate the presence of an error (figure 1, col. 3, lines 20-33, Helm et al.).

Byers et al. (US 5,416,362) teach that the present invention overcomes the disadvantages found in the prior art by providing a single enable line to provide signal transparency to a master/slave flip-flop. When the line is enabled the flip-flop macro is transparent and when the line is disabled the macro returns to the latching state as in a conventional bistable multivibrator (col. 1, line 64 to col. 2, line 2, Byers et al.).

Stewart et al. (US 4,464,754) teach a memory system in which two or more memory modules containing the same information have their respective data outputs connected to the same data line. Each module includes means for checking the parity of the data being read-out at its output and in the event of a parity error indication effectively disconnects its output from the data line (abstract, Stewart et al.).

However, the prior arts of record do not teach a circuit protected against transient disturbances comprising: a combinatory logic circuit having at least one output; a circuit for generating an error control code for said at least one output, said circuit for generating an error control code selected from a group of circuits consisting of a parity generation circuit and a circuit that is a duplicate of the combinatory logic circuit; and a memory element coupled to said circuit for generating an error control code and to said combinatory logic circuit, the memory element being controlled by the control code generation circuit to be transparent when the control code is correct, and to keep its state when the control code is incorrect; wherein said control code is correct when a parity generation circuit is used and when the output from the parity generation circuit is inactive, said control code being incorrect when the output from the parity generation circuit is active, and wherein said control code is correct when a duplicate of the combinatory logic circuit is used and when the out put from the duplicate of the combinatory logic circuit is identical to the output of the combinatory logic circuit, said control code being incorrect when the output from the duplicate of the combinatory logic circuit is not identical to the output of the combinatory logic circuit.

Hence, the prior arts of record do not anticipate nor render obvious the claimed inventions. Thus, claim 12 is allowable over the prior arts of record.

- Thus, claims 1-5, 9-10, 12 are allowable over the prior arts of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dipakkumar Gandhi
Patent Examiner

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100